Aditya Reddy

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EDUCATION

• Manipal University Jaipur, Jaipur, India Bachelor of Technology in Electronics and Communication Engineering 2024 – 2028 Jaipur, Rajasthan

Projects

Low Latency Trading Gateway | C++, FIX Protocol, Lock-Free Programming

GitHub Link

- Built a high-performance trading system in C++ with lock-free queues, memory pools, and CPU pinning to eliminate latency bottlenecks.
- Implemented zero-copy FIX protocol parsing using state machines and string views, achieving sub-2µs parser efficiency with 1.4µs average.
- Optimized tick-to-trade latency to 10-15 microseconds average with 2.8µs minimum, processing 400+ messages at 98% execution rate.

HTTP/1.1 Web Server | C, POSIX Sockets, Multithreading

GitHub Link

- Built a custom HTTP/1.1 server from scratch in C using raw POSIX sockets and a thread pool architecture, with zero external dependencies.
- Implemented full HTTP request parsing, static file serving, MIME type detection, and protection against directory traversal attacks.
- Benchmarked with ApacheBench: sustained 11.5K+ requests/sec and 8.7ms average latency under 100 concurrent clients.

Laplacian Edge Detection $\mid C$

GitHub Link

• Developed an image processing tool in C using the Laplacian operator to detect intensity discontinuities in grayscale images.

ACTIVITIES & EXTRACURRICULARS

- Qualified to penultimate round at Elicit Hacks 9.0 (MUJ),
- Completed the **Harvard CS50P Certificate** in Python programming, focusing on problem solving, data structures, and I/O systems.
- Volunteered at **Bison Asha School for Special Needs**, assisting in educational activities and organizing inclusive events over two years.

TECHNICAL SKILLS

- Languages: C/C++, Python, Verilog, SystemVerilog, Bash
- Developer Tools: Git, Make, Linux CLI, GCC, Shell scripting, LaTeX, GTKWave
- Technologies/Frameworks: Verilator, Icarus Verilog, RISC-V Toolchain, Vivado, GTKWave