Aditya Reddy

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Education

Manipal University Jaipur **Aug 2024 – May 2028**

Bachelor of Technology in Electronics and Communication Engineering *Jaipur, India*

- **Relevant Coursework:** Digital Logic Design, Circuit Analysis, Signals & Systems

Technical Skills

- **Hardware Description Languages:** Verilog, SystemVerilog
- **EDA & Simulation Tools:** Vivado, Verilator, GTKWave, LTspice
- **Programming:** C, C++, Python, RISC-V Assembly
- **Tools/Frameworks:** Git, Make, Linux, GCC, Shell Scripting, RISC-V Toolchain, FIX, STL, Docker, LaTeX

Projects

32-bit RISC-V Pipelined Processor | Verilog, GTKWave **GitHub Link**

- Designed 5-stage pipelined processor implementing RV32I instruction set with data forwarding and hazard detection logic
- Implemented branch prediction subsystem with 64-entry BTB, 2-bit saturating predictor, and 8-entry return address stack achieving 99.9% accuracy
- Built comprehensive testbench executing 4,998 instructions across all RV32I operation types, achieving 1.0 CPI and 0.2% pipeline stall rate on benchmarks
- Verified design through waveform analysis and instruction trace validation using GTKWave and Icarus Verilog

Low Latency Trading Gateway | C++, FIX Protocol, Lock-Free Programming **GitHub Link**

- Engineered high-performance trading gateway using lock-free queues and memory pools, reducing synchronization bottlenecks by 85%
- Implemented zero-copy FIX protocol parsing with state machines, achieving sub-2μs parsing with 1.4μs average latency
- Optimized tick-to-trade latency to 10–15μs average with 2.8μs minimum, sustaining 400+ messages at 98% execution rate
- Applied CPU pinning and cache-aligned memory allocation to eliminate scheduling delays and improve data locality

HTTP/1.1 Web Server | C, POSIX Sockets, Multithreading **GitHub Link**

- Architected custom HTTP/1.1 server in C with raw POSIX sockets and thread pool, eliminating external library dependencies
- Implemented complete HTTP request parsing, static file serving, and MIME type detection with directory traversal protection
- Achieved 11.5K+ requests/sec throughput with 8.7ms average latency under 100 concurrent clients using ApacheBench
- Designed connection pooling and keep-alive mechanisms to reduce TCP handshake overhead by 40%

Activities & Interests

- **Research Interests:** Computer Architecture, Low-Power VLSI Design, Hardware Acceleration, Digital Design Optimization, Networking Hardware
- Volunteered at Bison Asha School for Special Needs, supporting educational activities and organizing inclusive events (2022 – 2024)